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Paper

High Step-Down All-Passive Rectifier Derived Via Duality Principle from Cockcroft–Walton Circuit

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High step-down DC–DC converters and rectifiers are required for low-voltage, high-current applications. This paper proposes a high step-down all-passive rectifier to achieve this conversion. In particular, the proposed rectifier is derived via the duality principle from the N-stage Cockcroft–Walton circuit; the use of the duality principle in designing proposed rectifier is the novelty. In addition, the proposed rectifier is numerically analyzed based on its operation modes in the case of $N = 2$, 3, and 4. Furthermore, the validity of the two-stage rectifier designed via the proposed approach was experimentally verified as an example. © 2020 Institute of Electrical Engineers of Japan. Published by Wiley Periodicals LLC.

Keywords: high step-down; all-passive devices; duality principle; Cockcroft–Walton circuit

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1. Introduction

High step-down DC–DC converters and rectifiers are required to suitably transform high-voltage power from power sources for low-voltage, large-current applications, such as battery charging [1, 2].

Figure 1 (a) shows the general configuration for a transformer system used in low-voltage, large-current applications, which consists of a commercial power source, rectifier, high-frequency inverter, isolated transformer, rectifier, and step-down DC–DC converter. This system is controlled via three parameters, including duty of the high-frequency inverter, turn ratio of the isolated transformer, and step-down ratio of the DC–DC converter. Here, the high-frequency inverter provides a square voltage with adjusted by duty ratio.

For high step-down DC–DC converters, several topologies and control methods have been previously proposed [3–6]. Yao *et al.* [3] proposed a multiphase interleaved buck converter with additional coupled windings to achieve high-frequency, high step-down power transfer. Morales-Saldana *et al.* [4] deformed the buck converter and developed the quadratic buck converter with a single switch. Furthermore, Ki *et al.* [5] presented a high step-down transformerless single-stage single-switch AC/DC converter suitable for universal line applications; the topology integrates a buck-type power-factor correction cell with a buck-boost DC/DC cell wherein part of the input power is coupled to the output directly after processing. Palomo *et al.* [6] studied a family of quadratic step-down DC–DC converters connected in series or parallel. In particular, using their approach, the power transfer from the input port to output port is reduced on the interconnected converters when a non-cascading connection is used.

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Aside from DC–DC converters, rectifiers are also used as high step-down converters. Kutkut *et al.* [7] studied an improved full-bridge Zero Voltage Switching (ZVS) pulse width modulated (PWM) converter. They proposed including a current doubler rectifier on the secondary-side. The current doubler rectifier was subsequently applied to many applications [8, 9], and was further improved by several researchers. Xu *et al.* [10] integrated all the magnetic components into a single core and minimized the number of high current windings. In addition, they developed the current tripler DC–DC converter by applying the circuit topology of the current doubler rectifier to a three-phase transformer [11]. Wu *et al.* [12] and Antchev [13] used a coupled inductor as a current doubler rectifier in their works.

In ideal conditions, the high-frequency inverter and step-down DC–DC converter should be able to achieve high step-down gain with a considerably high duty ratio (Fig. 1(a)). However, in practice, the step-down gain is limited by the effects of the active switch, diode, and parasitic resistance of the inductor and capacitor. In addition, the high duty ratio leads to notable reverse-recovery problems as well as conduction losses. In fact, the isolated transformer shown in Fig. 1(a) could also achieve high step-down gain with a high turn ratio; nevertheless, this approach will also be affected by problems similar to those mentioned above.

Thus, in this study, I consider a high step-down all-passive rectifier, which integrates both a rectifier and step-down DC–DC converter, as shown in Fig. 1(b). Because the rectifier consists of passive devices, the system is highly reliable and efficient. However, the large size of the passive devices and non-control output value are the disadvantages of this system. In terms of system size, the system is able to overcome the problem at higher frequencies. Furthermore, compared with an all-passive rectifier, the high-frequency inverter responds accurately to load changes. To design the system depicted in Fig. 1(b), I focus on the high step-down all-passive rectifier. The contribution of the proposed rectifier is to use all passive devises. Since the active switches are not used, the proposed rectifier does not need the driving power and the proposed rectifier has high environmental friendliness and high reliability.

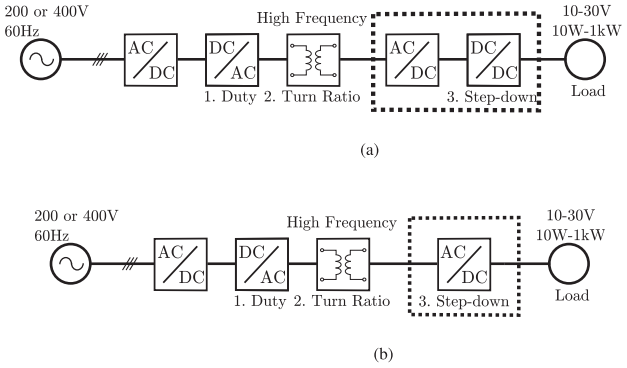

Fig. 1. System configuration for low-voltage and large-current application. (a) Conventional system; (b) Proposed system

The remainder of this paper is organized as follows. Section 2 presents the proposed rectifier, which is derived via the duality principle based on the Cockcroft–Walton (CW) circuit [14]. Section 3 discusses the operating principle for a two-stage rectifier obtained via proposed approach including the ideal operating conditions. The proposed circuit analysis results indicate that the proposed N-stage rectifier provides $2N$ times the current and $1/2N$ times the voltage compared with the input values. The novelty of my approach is the application of the duality principle to the N-stage CW circuit. Next, the operation of the proposed two-, three-, and four-stage rectifiers are numerically analyzed in Section 4. Then, In Section 5, the experimental details confirming the validity of the proposed two-stage rectifier are discussed. Finally, the conclusions are given in Section 6.

2. Proposed High Step-Down Passive Rectifier

2.1. Duality principle for circuits A circuit and its dual circuit have the same characteristics equation. Duality is obtained between the voltage and current sources, resistors and conductors, capacitors and inductors, and short and open circuits, among others, as listed in Table I.

The duality principle has been a widely used tool in the field of network theory, which, in itself, is a powerful tool for the development of new converter topologies. Because most power converters can be represented in several operating states, each with its own linear network representation; the first step is to find a dual network corresponding to each converter state [15]. Rabinovici *et al.* [16] presented current source schemes based on buck, boost, and buck-boost converters using the duality principle. Furthermore, DC–DC converters based on modified isolated transformers were obtained in a similar manner. Furthermore, Wolfs *et al.* [17] developed a new form of DC–DC converter by applying the duality principle to a half-bridge converter. Their proposed converter was intended for low-voltage source applications. In addition, they applied the duality principle to obtain a three-phase inverter using a center-tapped isolated transformer [18].

In this study, I apply the duality principle to the N-stage CW circuit [14]. The CW circuit is well-known as a high step-up rectifier. It has several advantages, such as simple construction and lack of active switches, i.e. it is an all-passive device. Thus, these advantages also exist for its dual circuit.

Table I. Duality relationship between circuit terms and components

Components and terms	↔	Dual of components and terms
Voltage source	↔	Current source
Resistor	↔	Conductor
Capacitor	↔	Inductor
Diode	↔	Diode
Switching device	↔	Switching device
Short circuit	↔	Open circuit
ON-time duty ratio	↔	OFF-time duty ratio
Series connection	↔	Parallel connection
Mesh or Loop	↔	Node
Inductor voltage second balance	↔	Capacitor ampere second balance
Star connection	↔	Delta connection

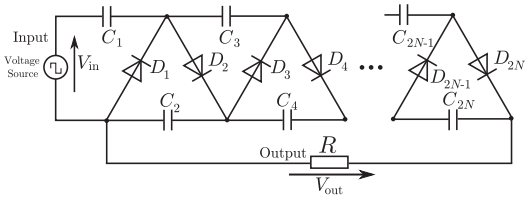

Fig. 2. Conventional N-stage Cockcroft–Walton circuit

2.2. Circuit configuration In this section, the circuit configuration of the proposed rectifier is presented. Figure 2 describes a conventional N-stage CW circuit, which consists of diodes and capacitors along with a voltage input source. The duality transformation can be directly applied to it. To obtain the network structure of the proposed rectifier, the following steps from [19] need to be followed. The result of this duality transformation is shown in Fig. 3.

(1) Consider a node in the middle of each loop of a conventional N-stage CW circuit.
(2) Mark a reference node away from all nodes outside the circuit: Fig. 3 draws the ellipse.
(3) Join the considered nodes, such that every line joining the nodes should pass through an element in the circuit.
(4) If the line drawn from the nodes is outside the circuit after passing through the circuit element, join the line with reference node.
(5) Replace each element with its dual pair element as listed in Table I.
(6) After replacing the existing elements with their dual elements, the polarity of the voltage source must be determined accordingly. If the loop current produced by the voltage source is positive, then, in the duality circuit, the current direction must be considered from the reference node to the associated node of the loop.

Figure 4 depicts the proposed rectifier obtained using the above mentioned steps. Because the proposed rectifier is derived from the

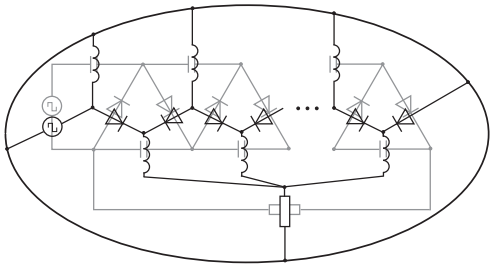

Fig. 3. Duality principle from N-stage Cockcroft–Walton circuit in Fig. 2

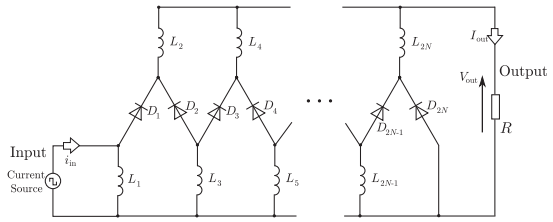

Fig. 4. Proposed high step-down all-passive rectifier from Fig. 3

conventional N-stage CW circuit in Fig. 2 by applying the duality principle, the output current increases by $2N$ times, while the output voltage is stepped-down by $1/2N$. As is clear from Fig. 4, the proposed N-stage rectifier consists of one current input source, $2N$ inductors, *viz*. L_1, L_2, ..., and L_{2N}, and $2N$ diodes, *viz*. D_1, D_2, ..., and D_{2N}. This rectifier can be employed to control the load as needed to achieve a low-voltage, large-current transfer.

3. Operating Principle

In this section, the operating principle of the proposed rectifier is described. To simplify circuit analysis, the following conditions are assumed.

- Number of stages is set to $N = 2$ in the example shown in Fig. 5.
- Current from the input source i_{in} is in the form of a square wave $\pm I_{\text{in}}$.
- Constant current I_{out} flows through the output load. Then, the output load is considered a constant current source to explain the operation modes.
- Inductors L_1, L_2, L_3, and L_4 have sufficiently large inductances, such that the inductor currents I_{L1}, I_{L2}, I_{L3}, and I_{L4} can be considered constant.
- Equivalent series resistances (ESRs) of the inductors L_1, L_2, L_3, and L_4 are neglected.
- Diodes D_1, D_2, D_3, and D_4 are assumed to be ideal, i.e. their ESRs and forward voltages are neglected.

In Mode 1, $i_{\text{in}} = -I_{\text{in}}$; Fig. 6(a) describes the current path in this mode. The input current source and inductor L_1 form a loop. The output current flows into the two branches: L_3–D_2–L_2 and D_4–L_4. Thus, the following equations hold:

$$I_{L1} = I_{\text{in}} \tag{1}$$

$$I_{L2} = I_{L3} \tag{2}$$

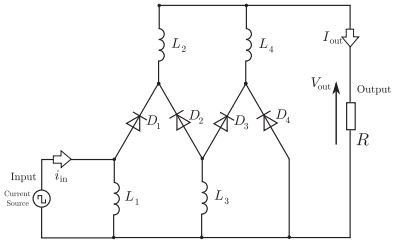

Fig. 5. Proposed high step-down all-passive rectifier at $N = 2$ in Fig. 4

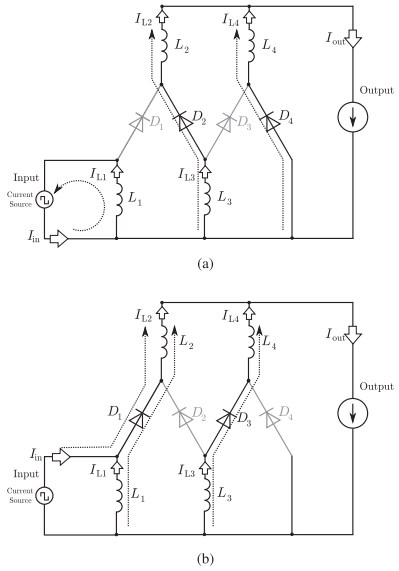

Fig. 6. Operation modes of the proposed rectifier in Fig. 5. (a) Mode 1 ($i_{\text{in}} = -I_{\text{in}}$); (b) mode 2 ($i_{\text{in}} = +I_{\text{in}}$)

$$I_{\text{out}} = I_{L2} + I_{L4} \tag{3}$$

In Mode 2, $i_{\text{in}} = +I_{\text{in}}$; Fig. 6(a) describes the current path in this mode. Here, the sum of the input current I_{in} and inductor current I_{L1} flows through the diode D_1. In addition, the presence of inductor current, I_{L3}, leads to a change in the current path from D_2 to D_3 in the circuit. Thus, the following equations hold:

$$I_{L2} = I_{\text{in}} + I_{L1} = 2I_{\text{in}} \tag{4}$$

$$I_{L4} = I_{L3} = I_{L2} = 2I_{\text{in}} \tag{5}$$

$$I_{\text{out}} = I_{L2} + I_{L4} = 4I_{\text{in}} \tag{6}$$

Based on [6], the proposed two-stage rectifier provides a current four times that of I_{in}, which is the amplitude of the input current. Furthermore, in terms voltage, the proposed rectifier steps the voltage down to one-fourth that of the input voltage. Although a two-stage rectifier was considered as the example in this section, the operating principle for the dual N-stage CW circuit can be described in the same manner. Therefore, a dual N-stage CW circuit is expected to have a current output $2N$ times that of the input current and voltage output $1/2N$ times that of the input voltage.

4. Numerical Analysis

I verify the performance of the rectifier built using the proposed approach via numerical analysis. A circuit simulator, PLECS, was used for the numerical analysis.

4.1. Conditions As discussed previously, the input for the proposed rectifier is regarded as a current source, because it is the dual component for the voltage source in the conventional rectifier design. However, in practice, the input source will, in fact, be a voltage source. Therefore, here, I set a voltage source as the input source of Fig. 4.

Next, the parameters in Fig. 4 are set as follows:

- Number of stages: N=2, 3, and 4,
- Inductance of all inductors: Variable,
- ESR of the all inductors: 25 mΩ,
- Input voltage source v_{in} provides a square wave $\pm V_{\mathrm{in}}$[*],
- Amplitude of v_{in}: $V_{\mathrm{in}} = 120$ V,
- Frequency of the input voltage source: $f = 100$ kHz,
- Forward voltage of all diodes: $V_{\mathrm{f}} = 1.0$ V,
- Conduction resistance of the all diodes: $R_{\mathrm{don}} = 22$ mΩ.

4.2. Inductor size analysis This section analyzes the inductor size in the proposed rectifier. Figure 7 shows the V_{out} characteristics using the variable inductor L in the proposed rectifier for different number of stages at $R = 10$, 20, 50, and 100 Ω. The proposed rectifier operates CCM presented in the Section 3 when the inductor L is large enough. On the other hand, when the inductor L is small, the proposed rectifier operates DCM, so the output voltage is not stepped down. From Fig. 7(d), the inductor L in the two-stage proposed rectifier should be more than 3 mH.

4.3. Output power characteristics This section set the inductor L= 5 mH[†] from the previous subsection.

Figure 8 shows the V_{out}–P_{out} characteristics for the proposed rectifier for different number of stages. In the case of $N = 2$, as mentioned previously, the proposed two-stage rectifier provides a step-down to one-fourth for voltage. Thus, the ideal voltage will be 120/4 = 30 V. In addition, because the proposed rectifier also includes the forward voltage of all diodes $V_{\mathrm{f}} = 1.0$ V, the ideal voltage is calculated to be 29 V. From this result for $N = 2$, there are three conditions for output voltage with respect to the load: middle-load, large-load, and light-load. In addition, the output voltage has two points for output power in the results. The reason is that the load resistance is different. As the load resistance value decreases, the output voltage and power also decrease. As a result, the results curve.

The operation for each condition is explained based on the results of $N = 2$ in Fig. 8. For the middle-load condition: between 5 and 500 W; the proposed rectifier achieves the operation, which is explained in the previous section. In fact, the output voltage retains the ideal value of 29 V.

[*] In the actual system, such as Fig. 1, the input side consists of an high-frequency inverter and transformer. Therefore, the input power supply can be regarded as a square wave voltage source.

[†] To satisfy CCM, a large inductor is required. However, the theoretical relational expression has not been clarified yet. Then, the theoretical analysis is left for the future work.

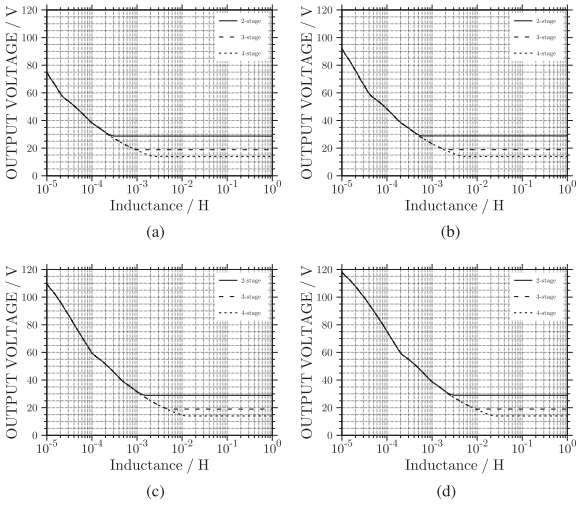

Fig. 7. V_{out}-L characteristics in proposed rectifier with voltage source at load resistor R = 10, 20, 50, and 100 Ω. (a) $R = 10\,\Omega$; (b) $R = 20\,\Omega$; (c) $R = 50\,\Omega$; (d) $R = 100\,\Omega$

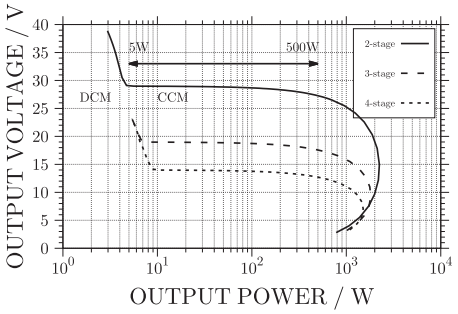

Fig. 8. V_{out}-P_{out} characteristics in proposed rectifier with voltage source

For the large-load condition: more than 500 W; the output voltage decreases as the output power increases. This phenomenon is typically observed with general rectifiers, and can be attributed to the ESRs of the inductors as well as the conduction resistances of the diodes.

For instance, the output current I_{out} is 40 A at P_{out}= 1 kW and V_{out}= 25 V. The output current always flows through two inductors and one diode as shown in Fig. 6. The results suggest that inductors with ESRs of less than 25 m Ω and diodes with conduction resistances of less than 22 m Ω must be used for the proposed rectifier design for large-load conditions.

For the light-load condition: less than 5 W; the output voltage sharply increases with respect to the load. For light-load conditions, the inductor current is not sufficient to realize the rectification operation using the proposed rectifier design. In fact, the input current is roughly calculated for the loop of the inductor L_1 and voltage source v_{in} by ignoring the ESR of the inductor L_1. Here, the following equations hold:

$$L\frac{di_{L1}}{dt} = \pm V_{\mathrm{in}} \tag{7}$$

$$i_{L1} = \frac{V_{\mathrm{in}}}{L}t + i_{\mathrm{in}}(0) \quad \left(0 \le t \le \frac{T}{2}\right) \tag{8}$$

$$i_{L1} = -\frac{V_{\text{in}}}{L}\left(t - \frac{T}{2}\right) + i_{L1}\left(\frac{T}{2}\right) \quad \left(\frac{T}{2} \le t \le T\right) \tag{9}$$

where $T = 1/f$ denotes the period of the input voltage v_{in}. At the bounding condition between continuous current mode (CCM) and discontinuous current mode (DCM), the $i_{\text{L1}}(0)$ is equal to 0 and average of $i_{\text{L1}}(t)$ becomes $I_{\text{L1}} = V_{\text{in}}/4fL$. From [6], I_{out} boosts four times I_{L1}: $I_{\text{out}} = V_{\text{in}}/fL$. The output power P_{out} is roughly estimated as: $V_{\text{out}}V_{\text{in}}/fL \approx 7$ W. For that reason, the proposed rectifier cannot maintain the CCM in the light-load region. Furthermore, because the output voltage responds sensitively to the load, the light-load region should be avoided during the rectifier design stage. However, if the proposed rectifier has to be used at light-load conditions, the inductance must be sufficiently high.

Based on the numerical analysis described above, it is clear that the proposed rectifier is effective as a step-down voltage rectifier in the middle-load region.

The results for the three- and four-stage rectifiers based on the proposed design and shown in Fig. 8 also indicate a similar trend to the previously described two-stage rectifier. The output voltage $V_{\text{in}}/2N - V_{\text{f}}$ maintains the rectifier in the middle-load region. As the number of stages N increases, the number of inductors through which the current flows also increases. Then, the limitation of the middle-load region is narrowing with respect to N.

Furthermore, the performance of the proposed rectifier is verified based on efficiency η, which is defined as $\eta = P_{\text{out}}/P_{\text{in}}$, and on the total power factor (TPF). Figure 9(a), (b) shows the η-P_{out} and TPF-P_{out} characteristics for the proposed rectifier design. In particular, the efficiency η is maintained at more than 0.9 at power outputs of less than 500 W in case of $N = 2$. Thus, the proposed rectifier achieves high efficiency over a wide range of power. However, the efficiency η decreases as the number of stages N increase. This is because the ESRs of the inductors and conduction resistances of the diodes affect η. η can be improved by using inductors with ESRs of less than 25 m Ω and diodes with conduction resistances of less than 22 m Ω even when the proposed rectifier is used at large-load conditions.

The TPF is significantly affected by the input current waveform. When the output power is sufficiently large, the input current maintains a square wave form, as shown in Fig. 6. In contrast, when the output power decreases, the input current includes the ripple from [8] to [9]. Thus, to design the proposed rectifier for Fig. 1(b), it is necessary to consider the effect from this current ripple.

5. Experimental Verification

In this section, the experimental verification procedure for the proposed rectifier is discussed. For the experiment, the prototype of the proposed rectifier consists of two stages. Here, the case of three and four stages of the proposed rectifier is left for future work. Based on the numerical results presented in Section 4, the output power is set around 30 W because the proposed rectifier operates in the CCM and with high efficiency at that power.

5.1. Experimental conditions The devices and their associated parameters used in the experiment are as follows:

- Inductance of all inductors: L= 10 mH,[‡]

[‡] They are custom made by UNION Electric Co.,Ltd.. The size is 125 W × 78D × 120H, 2.8 kg.

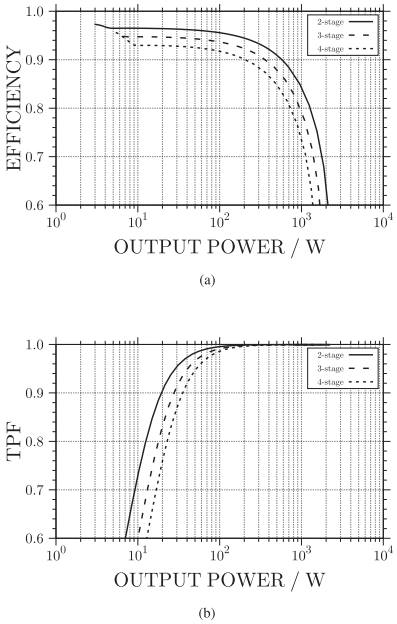

Fig. 9. η-P_{out} and TPF-P_{out} characteristics in proposed rectifier. (a) η-P_{out}; (b) TPF-P_{out}

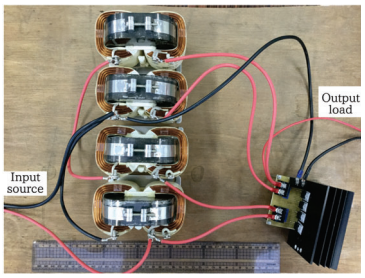

Fig. 10. Photo of the prototype rectifier

- input voltage source v_{in} provides a square wave $\pm V_{\text{in}}$ from a bipolar power supply HSA4051,
- amplitude of v_{in}: $V_{\text{in}} = 120$ V,
- frequency of the input voltage source: $f = 100$ kHz,
- all diodes: SiC SBD, SCS205KG (1200 V, 5 A).
- output load: $R = 22\Omega$,
- output smoothing capacitor: 10 μF.

Figure 10 shows the photo of the prototype rectifier in this section.

5.2. Experimental results Figure 11 shows the input and output waveforms in proposed dual two-stage CW rectifier. From these experimental results, it was confirmed that the proposed rectifier provide about one-fourth times the voltage and four times the current at the output load compared with the input source, which is in agreement with the values obtained based on the operating principle, as described in Section 3.

Furthermore, the performance of the proposed rectifier in terms of η and TPF is 0.922 and 0.839, respectively, as obtained from a power meter PA4000, made in Tektronix.

The experimental results in this paper verify the operating principle. The size of the inductors and their comparison are left for the future works. The results show the high TPF in the proposed

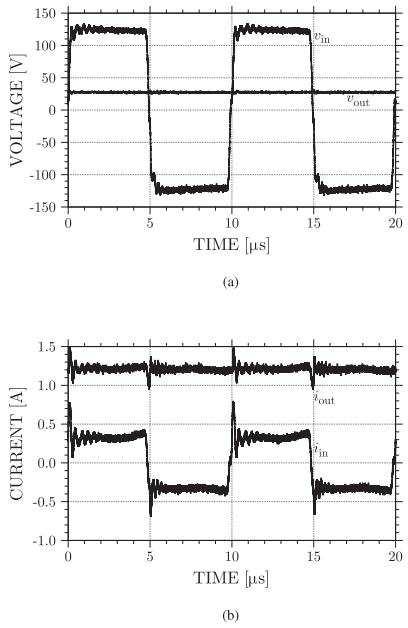

Fig. 11. The input and output waveforms in proposed rectifier. (a) Voltage waveforms; (b) current waveforms

rectifier as the input voltage and current waveforms are almost square. However, TPF in the original CW circuit is very low because the input current of the original CW circuit flows like a spike in a short time. In this case, the input power supply may have a built-in filter inside for supplying a square wave voltage. Then, the proposed rectifier should be verified the operation when using an inverter as the input source. The prototype test is left for the future work.

6. Conclusions

In this study, I investigated a novel high step-down all-passive rectifier design. The proposed rectifier is derived via the duality principle from the N-stage CW circuit. I considered a two-stage rectifier based on the proposed design to analyze the different operation modes. In particular, I numerically and experimentally verified the validity of the proposed rectifiers. The results indicate that the proposed rectifier realizes step-down voltage with high efficiency over a wide power range. The novelty of my approach is the application of the duality principle to the N-stage CW circuit.

In future work, I plan to prototype the system in Fig. 1 consisting of a high-frequency inverter, an isolated transformer, and the proposed rectifier to verify its working principle and usefulness.

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